UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,107,502 B2
APPLICATION NO. : 10/767046
DATED : September 12, 2006
INVENTOR(S) : Todd Michael Burdine

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page 1, Col. 1, Line Item (57), should read as follows:

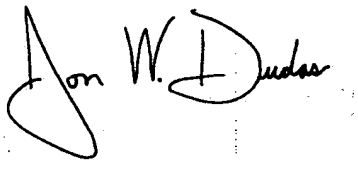
ABSTRACT

Methods of testing scan chains in integrated circuits are provided. One method may include steps of placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain, placing the scan chain circuit into a failing region, applying a shift clock pulse to the L2 (slave) latch, placing the scan chain circuit into an operating region, and unloading the scan chain. An additional step may be added to analyze the resulting data. Another method may include the steps of, placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain circuit, placing the scan chain circuit into a failing region, applying a scan clock pulse to the L1 (master) latch, placing the scan chain circuit into an operating region, applying a shift clock pulse to the L2 latch, and unloading the scan chain. An additional step may be added to analyze the resulting data.

22 Claims, 10 Drawing Sheets

Signed and Sealed this

Twenty-seventh Day of March, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office